



***ATJ2111A***

***Product Datasheet***

*Latest Version: 1.1*

---

*2008-07-11*

## *Declaration*

---

Circuit diagrams and other information relating to products of Actions Semiconductor Company, Ltd. ("Actions") are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction is not necessarily given. Although the information has been examined and is believed to be accurate, Actions makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and disclaims any responsibility for inaccuracies. Information in this document is provided solely to enable use of Actions' products. The information presented in this document does not form part of any quotation or contract of sale. Actions assumes no liability whatsoever, including infringement of any patent or copyright, for sale and use of Actions' products, except as expressed in Actions' Terms and Conditions of Sale for. All sales of any Actions products are conditional on your agreement of the terms and conditions of recently dated version of Actions' Terms and Conditions of Sale agreement Dated before the date of your order.

This information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights, copyright, trademark rights, rights in trade secrets and/or know how, or any other intellectual property rights of Actions or others, however denominated, whether by express or implied representation, by estoppel, or otherwise.

Information Documented here relates solely to Actions products described herein supersedes, as of the release date of this publication, all previously published data and specifications relating to such products provided by Actions or by any other person purporting to distribute such information. Actions reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your Actions sales representative to obtain the latest specifications before placing your product order. Actions product may contain design defects or errors known as anomalies or errata which may cause the products functions to deviate from published specifications. Anomaly or "errata" sheets relating to currently characterized anomalies or errata are available upon request. Designers must not rely on the absence or characteristics of any features or instructions of Actions' products marked "reserved" or "undefined." Actions reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Actions' products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal

---

injury or severe property damage. Any and all such uses without prior written approval of an Officer of Actions and further testing and/or modification will be fully at the risk of the customer.

Copies of this document and/or other Actions product literature, as well as the Terms and Conditions of Sale Agreement, may be obtained by visiting Actions' website at <http://www.actions-semi.com/> or from an authorized Actions representative. The word "ACTIONS", the Actions' LOGO, whether used separately and/or in combination, and the phase "ATJ2111A", are trademarks of Actions Semiconductor Company, Ltd., Names and brands of other companies and their products that may from time to time descriptively appear in this product data sheet are the trademarks of their respective holders; no affiliation, authorization, or endorsement by such persons is claimed or implied except as may be expressly stated therein.

**ACTIONS DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE.**

**IN NO EVENT SHALL ACTIONS BE RELIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF ACTIONS OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER ACTIONS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES OR NOT.**

#### Additional Support

Additional product and company information can be obtained by visiting the Actions website at: <http://www.actions-semi.com>

## *Contents*

---

<b>Declaration</b>	<b>2</b>
<b>Contents</b>	<b>4</b>
<b>List of Figures</b>	<b>6</b>
<b>List of Tables</b>	<b>7</b>
<b>Revision History</b>	<b>8</b>
<b>1 Introduction</b>	<b>9</b>
<b>2 Pin Description</b>	<b>11</b>
2.1 Pin Assignment	11
2.2 Pin Definition	12
<b>3 Function Description</b>	<b>15</b>
3.1 Functional Block Diagram	15
3.2 MCU Core	16
3.2.1 MCU System Memory Mapping	16
3.3 DSP24 Core	17
3.4 ZRAM1, ZRAM2 and ZRAM3	17
3.5 USB2.0 SIE	18
3.6 NAND Flash /SMC Controller	18
3.7 Key Scan Interface	19
3.8 General Purpose IO Ports	19
3.9 HOSC/PLL	20
3.10 PMU/DC-DC	20
3.10.1 DC-DC converters and regulators	20
3.10.2 Battery monitor	20
3.11 A/D, D/A, IIS Port and Headphone Driver	21
3.11.1 D/A Interface	21

---

---

3.11.2	A/D.....	21
<b>4</b>	<b>Electrical Characteristics.....</b>	<b>23</b>
4.1	Absolute Maximum Ratings.....	23
4.2	Capacitance .....	23
4.3	DC Characteristics .....	23
4.4	AC Characteristics.....	24
4.4.1	AC Test Input Waveform .....	24
4.4.2	AC Test Output Measuring Points.....	25
4.4.3	Reset Parameter.....	25
4.4.4	Initialization Parameter .....	25
4.4.5	GPIO Interface Parameter .....	26
4.4.6	Ordinary ROM Parameter .....	27
4.4.7	External System Bus Parameter .....	28
4.4.8	Bus Operation.....	29
4.4.9	A/D Converter Characteristics.....	29
4.4.10	Headphone Driver Characteristics Table.....	30
4.4.11	LCM Driver Parameter .....	31
<b>5</b>	<b>Soldering Conditions.....</b>	<b>33</b>
5.1	Recommended Soldering Conditions.....	33
5.2	Precaution against ESD for Semiconductors .....	33
5.3	Handling of Unused Input Pins for CMOS .....	34
5.4	Status before Initialization of MOS Devices .....	34
<b>6</b>	<b>ATJ2111A Package Drawing.....</b>	<b>35</b>
<b>7</b>	<b>Appendix.....</b>	<b>36</b>
7.1	Acronym and Abbreviations .....	36

## *List of Figures*

---

Figure 1: ATJ2111A Pin Out Figure.....	11
Figure 2: ATJ2111A Functional Block Diagram .....	15
Figure 3: MCU System Memory Mapping .....	16
Figure 4: Key Scan Timing .....	19
Figure 5: D/A Block Diagram .....	21
Figure 6: AC Test Waveform .....	25
Figure 7: AC Test Output Measuring Points .....	25
Figure 8: Reset Parameter.....	25
Figure 9: Initialization .....	26
Figure 10: Input Level Width .....	26
Figure 11: Output Rise/Fall Time .....	26
Figure 12: Output Level Width .....	27
Figure 13: Ordinary ROM.....	27
Figure 14: External System Bus Parameter.....	28
Figure 15: Memory Read Timing .....	29
Figure 16: Memory Write Timing .....	29
Figure 17: Frequency Response Diagram of Headphone Driver .....	31
Figure 18: THD + N Amplitude Diagram of Headphone Driver .....	31
Figure 19: LCM Interface Timing .....	32
Figure 20: ATJ2111A Package Drawing .....	35

## *List of Tables*

---

Table 1: ATJ2111A Pin Definition .....	12
Table 2: GPIO Modes.....	19
Table 3: Power mode configuration .....	20
Table 4: Relationship between Battery Type and A/D Input Range.....	21
Table 5: Absolute Max Ratings.....	23
Table 6: Capacitance .....	23
Table 7: DC Characteristics .....	23
Table 8: Reset Parameter .....	25
Table 9: Initialization Parameter.....	25
Table 10: GPIO Interface Parameter .....	26
Table 11: Ordinary ROM Parameter .....	27
Table 12: External System Bus Parameter.....	28
Table 13: A/D Converter Characteristics .....	30
Table 14: Headphone Driver Characteristics .....	30
Table 15: LCD Driver Parameter .....	32
Table 16: Soldering Conditions for Surface-Mount Devices .....	33

## *Revision History*

---

Date	Revision	Description
2008-03-14	1.0	Initial Release;
2008-07-11	1.1	1. GPIO driver updated 2. Some description modified



# 1

## Introduction

---

### Overview

The ATJ2111A is a single-chip highly-integrated digital music system solution for devices such as dedicated audio players. It includes an audio decoder with a high performance DSP with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. ATJ2111A also provides an interface to flash memory, LED/LCD, button and switch inputs, headphones, and microphone, and FM radio input and control. Its programmable architecture supports WMA and other digital audio standards. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. The Chip has low power consumption to allow long battery life and efficient flexible on-chip DC-DC converters that allows 1xAA and 1xAAA. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. The A/D includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players.

### Features

- MPEG1/2/2.5 Audio Layer 1,2,3 decoder, bit rate 8-448Kbps,8-48KHz,CBR/VBR
- Support WMA Decoder, bit rate 32-384Kbps,8-48KHz
- Digital Voice Recording at ultra low 4.4 or 8Kbps w/ Actions Speech Algorithm
- 24 bits DSP Core
- On-chip DSP PM with SRAM(16K\*24), can be switched to be MCU memory space
- On-chip DSP DM with SRAM(16K\*24), can be switched to be MCU memory space
- Integrated MCU, the instruction set is compatible with Z80
- Internal ZRAM1((16K-64)\*8),ZRAM2((12K+256)\*8),ZRAM3(16K\*8) accessed by MCU
- Internal 14Kx8 BROM build in Boot up and USB Upgrade firmware
- Internal (21K+12K)x8 TROM
- Internal SRAM access time<7ns, MROM access time<16ns
- External up to 4(pcs)x 32M~4G bytes Nand type Flash accessed by MCU or DMA
- Support 24MHz OSC with on-chip PLL for DSP and about 32KHz RC oscillator
- 2-channel DMA,1-channel CTC and interrupt controller for MCU
- Energy saving with dynamic power management, supporting cell only

- Support USB2.0 Compliance PHY+SIE,RD/WR:6MB/5MB(NAND Flash Base)
- Build in Stereo 20-bit Sigma-Delta D/A
- Build in Key Scan Circuit and GPIO
- Support external 8080 Series LCM driver interface
- Support FM Radio input and 32 levels volume control
- Support Stereo 21-bit Sigma-Delta A/D for Microphone/FM Input, sample rate at 8/12/16/22/24/32/48KHz
- MCU run at 48MHz(typ),F/W can program from DC up to 48MHz transparently
- DSP+PM/DM Speed up to 90MIPS,while 48mips@1.6v
- D/A+PA SNR :without A weight>91dB
- A/D SNR >86dB
- Headphone driver output 2x20Mw @16ohm
- Standby Leakage Current: VCC:50uA@3.0V(MAX), VDD: 350uA@1.6V(MAX)
- Low Power Consumption : <80mW@1.6V at typical WMA decoder solution
- Package at LQFP-64 (10x10mm)

## 2

## Pin Description

### 2.1 Pin Assignment

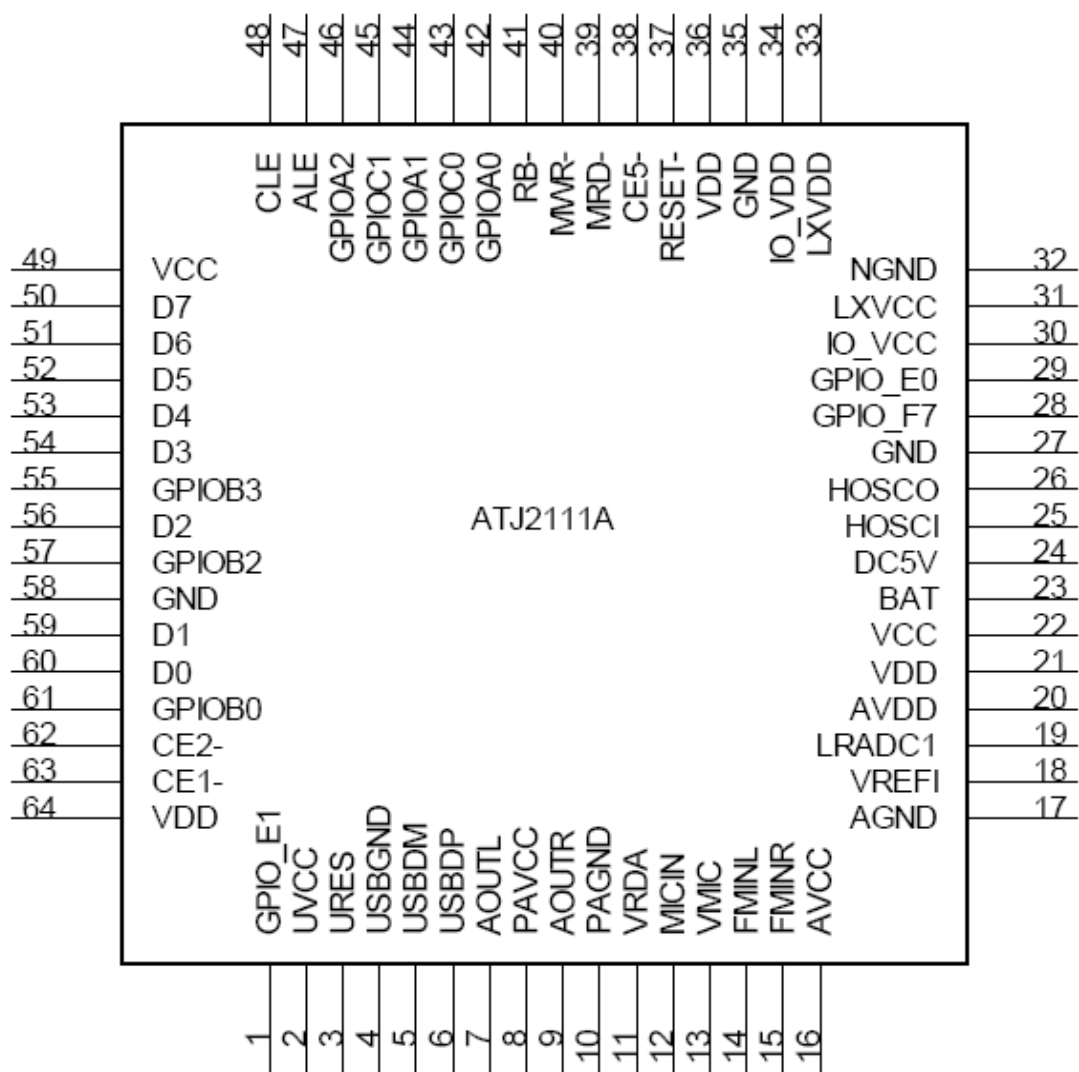


Figure 1: ATJ2111A Pin Out Figure

## 2.2 Pin Definition

Table 1: ATJ2111A Pin Definition

Pin No.	Pin Name	I/O Type	Driver	Reset Default	Short Description
1	GPIO_E1	BI	5mA	Z	Bit1 of General purpose I/O port E
	KEYI3	I		Z	Bit3 of key scan input3
2	UVCC	PWR	/	/	Power supply for USB
3	URES	AO	/	/	USB precision Resistor
4	USBGND	PWR	/	/	USB ground
5	USBDM	A	/	H	USB data minus
6	USBDP	A	/	H	USB data plus
7	AOUTL	AO	/	/	Int. PA left channel analog output
8	PAVCC	PWR	/	/	Power supply for power amplifier
9	AOUTR	AO	/	/	Int. PA right channel analog output
10	PAGND	PWR	/	/	Power amplifier ground
11	VRDA	AO	/	/	Bypass capacitor connect pin for Int. D/A Reference voltage
12	MICIN	AI	/	/	Microphone pre-amplifier input
13	VMIC	PWR	/	/	Power supply for Microphone
14	FMINL	AI	/	/	Left channel of FM line input
15	FMINR	AI	/	/	Right channel of FM line input
16	AVCC	PWR	/	/	power supply of Analog
17	AGND	PWR	/	/	Analog ground
18	VREFI	AI	/	/	Voltage reference input
19	LRADC1	AI	/	/	Low resolution A/D input 1
20	AVDD	PWR	/	/	Analog Core power pin
21	VDD	PWR	/	/	Digital Core power
22	VCC	PWR	/	/	Digital power pin
23	BAT	I	/	/	Battery Voltage input.
24	DC5V	AI	/	/	5.0V Voltage
25	HOSCI	AO	/	/	High frequency crystal OSC input

26	HOSCO	AI	/	/	High frequency crystal OSC output
27	GND	PWR	/	/	Ground
28	GPIO_F7	BI	10mA	Z	Bit7 of General purpose I/O port F
29	GPIO_E0	BI	5mA	Z	Bit0 of General purpose I/O port E
	KEY12	I		/	Bit2 of key scan input
30	IO_VCC	PWR	/	/	IO for VCC DC-DC
31	LXVCC	PWR	/	/	VCC DC-DC pin
32	NGND	PWR	/	/	NMOS Ground
33	LXVDD	PWR	/	/	VDD DC-DC pin
34	IO_VDD	PWR	/	Z	IO for VDD DC-DC
35	GND	PWR	/	/	Ground
36	VDD	PWR	/	/	Digital Core power
37	RESET-	I	/	H	System reset input (active low)
38	CE5-	O	10mA	H	Ext. memory chip enable 5
	GPIO_A3	BI		/	Bit3 of General purpose I/O port A
39	MRD-	O	/	H	Ext. memory read strobe
40	MWR-	O	/	H	Ext. memory write strobe
41	RB-	I	/	H	Nand Type flash Ready/Busy status input.
42	GPIO_A0	O	5mA	Z	Bit0 of General purpose I/O port A
43	GPIO_C0	BI	5mA	OD	Bit0 of General purpose I/O port C
	I2C_SCL	O		/	I2C serial clock (Open drain)
44	GPIO_A1	O	5mA	Z	Bit1 of General purpose I/O port A
45	GPIO_C1	BI	5mA	OD	Bit1 of General purpose I/O port C
	I2C_SDA	O		/	I2C Serial data (Open drain)
46	GPIO_A2	O	5mA	Z	Bit2 of General purpose I/O port A
47	ALE	O	/	L	Address latch enable for NAND flash
48	CLE	O	/	L	Command latch enable for NAND flash
49	VCC	PWR	/	/	Digital power pin
50	D7	BI	/	L	Bit7 of ext. memory data bus
51	D6	BI	/	L	Bit6 of ext. memory data bus

52	D5	BI	/	L	Bit5 of ext. memory data bus
53	D4	BI	/	L	Bit4 of ext. memory data bus
54	D3	BI	/	L	Bit3 of ext. memory data bus
55	GPIO_B3	BI	15mA	Z	Bit3 of General purpose I/O port B
	KEY01	O		/	Bit1 of key scan circuit output
	SIRQ-	I		/	Ext. interrupt request input
56	D2	BI	/	L	Bit2 of ext. memory data bus
57	GPIO_B2	BI	5mA	Z	Bit2 of General purpose I/O port B
	CE4-	O		H	External MROM Chip enable 4
	KEY00	O		/	Bit0 of key scan circuit output
58	GND	PWR	/	/	Ground
59	D1	BI	/	L	Bit1 of ext. memory data bus
60	D0	BI	/	L	Bit0 of ext. memory data bus
61	GPIO_B0	BI	5mA	Z	Bit0 of General purpose I/O port B
	CE3-	O		H	CE3- of NAND Flash
	KEY10	I		H	Bit0 of key scan circuit input
62	CE2-	O	5mA	H	Ext. memory chip enable 2
	GPIO_A4	BI		/	Bit4 of General purpose I/O port A.
63	CE1-	O	/	H	Ext. memory chip enable 1
64	VDD	PWR	/	/	Digital Core power

**NOTE:**

- 1: PWR—Power Supply
- 2: AI—Analog Input
- 3: AO—Analog Output
- 4: O—Output
- 5: I—Input
- 6: BI—Bidirection

3

Function Description

3.1 Functional Block Diagram

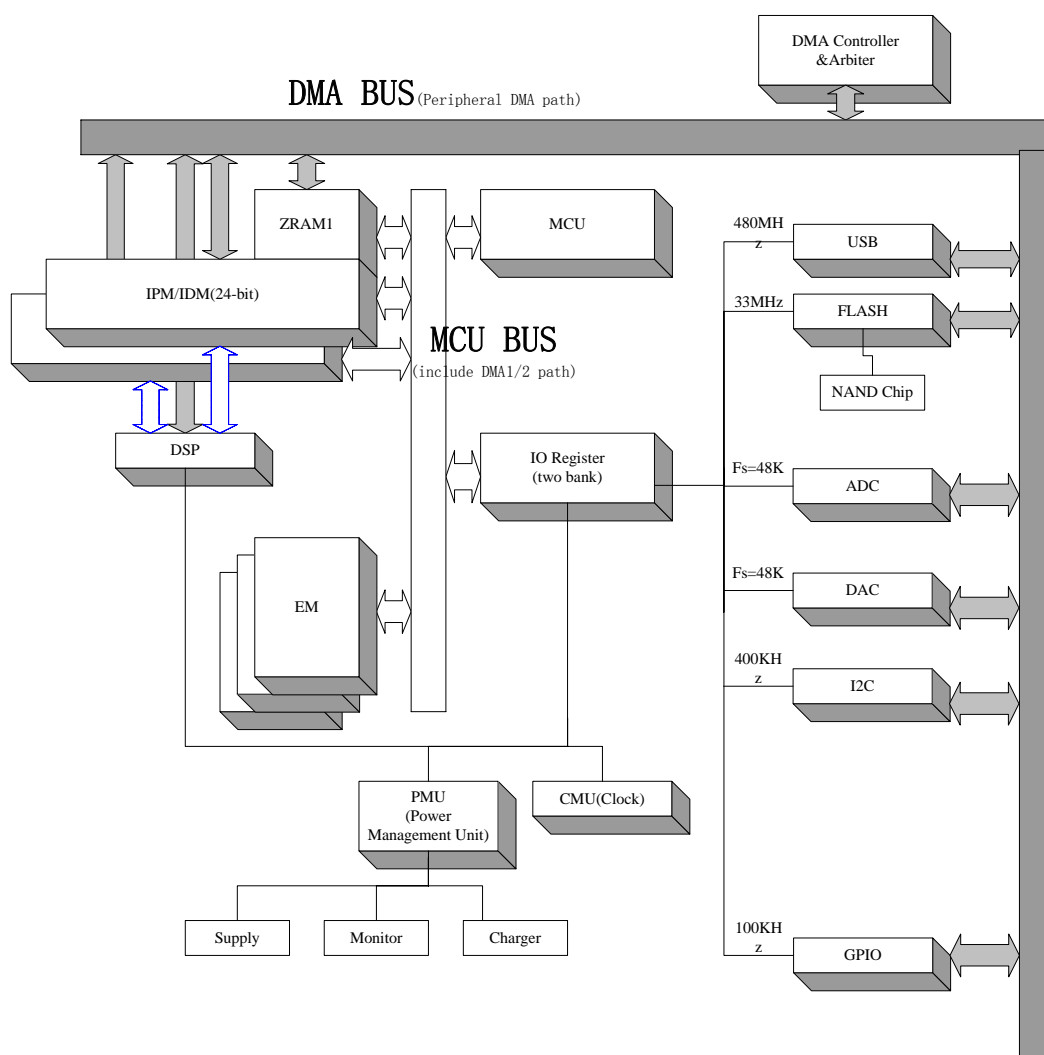
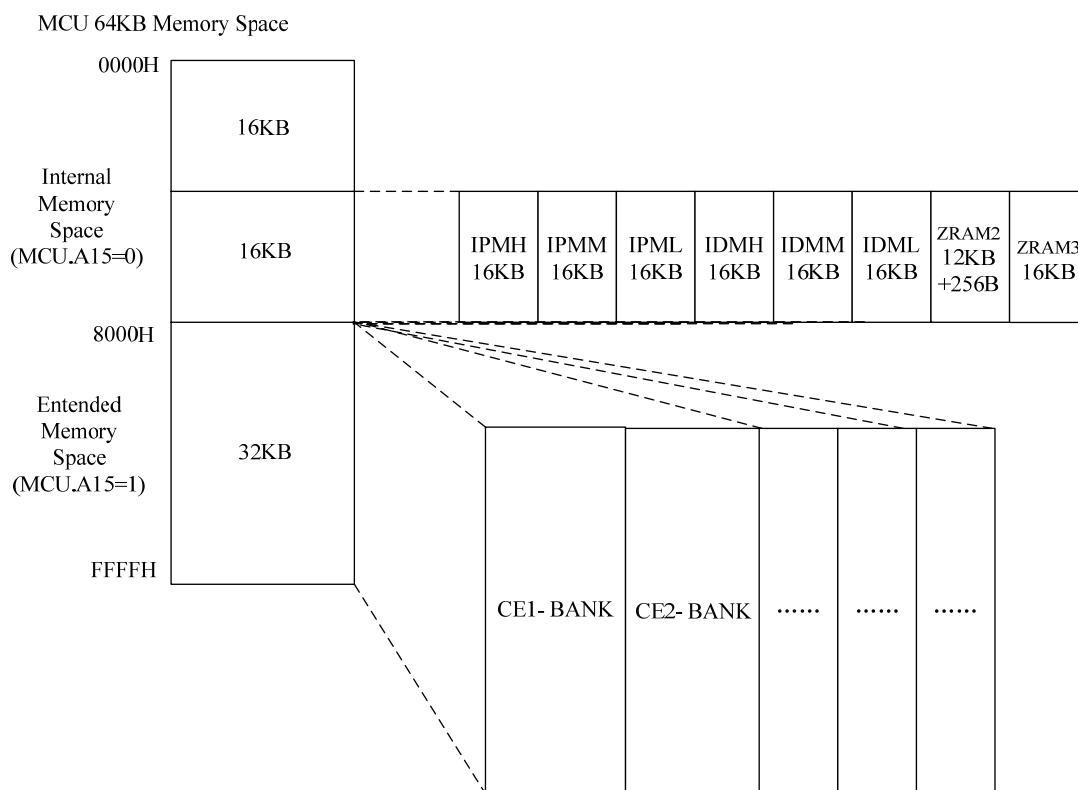


Figure 2: ATJ2111A Functional Block Diagram

## 3.2 MCU Core

### 3.2.1 MCU System Memory Mapping



**Figure 3: MCU System Memory Mapping**

#### **Internal MCU MROM/SRAM memory mapping:**

- 1) (16K-64)byte ZRAM1(IA15=0,IA14=0) : 0000H-3FBFH
- 2) 8Kbyte B1+B2(IA15=0,IA14=1,IOReg05.[2:0]=111): 4000H-5FFFH
- 3) (4K+256) byte URAM: 6000H-70FFH, it has synchronization and asynchronism accessing modes.
- 4) 16Kbyte ZRAM3(IA15=0,IA14=1,IOReg05.[2:0]=011): 4000H-7FFFH
- 5) 14Kbyte BROM(IA15=1,Reg02=00h, Reg01=00h) : 8000h-B7FFh
- 6) 21Kbyte TROM1(IA15=1,Reg02=00h,Reg01=02h) : 8000h-D3FFh
- 7) 12Kbyte TROM2(IA15=1,Reg02=00h,Reg01=03h) : 8000h-AFFFh



**Internal DSP IPM/IDM memory mapping:**

- 1) 16K x24bit IPM SRAM : 0000H-3FFFH
- 2) 16K x24bit IDM SRAM : 0000H-3FFFH

**Internal DSP IPM/IDM memory mapping accessed by MCU:**

- 1) 16K x3 byte IPM SRAM : 4000H-7FFFH
- 2) 16K x3 byte IDM SRAM : 4000H-7FFFH

(Hi/Mid/Low Byte Select and Mapping Mode controlled by IOReg05)

**DMA MODE NOTE:**

- 1: When DMA1 and DMA2 are active, MCU will halt, while DMA1 and DMA2 have priority.
- 2: FLASHDMA or USB DMA is active, MCU will not halt.

### 3.3 DSP24 Core

This Core is a high performance, programmable Digital Signal Processor (DSP) suitable for a variety of digital audio compounding functions, such as Dolby AC-3 Surround which require large memory provided and the higher accuracy. RDSP24 is a general purpose DSP which can be appended various peripherals circuitry to implement some advanced signal processing algorithms for audio application.

### 3.4 ZRAM1, ZRAM2 and ZRAM3

Speed: max read time 30 ns from ZRAMRD- going low

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

ZRAM2 is composed of B1,B2 and URAM: 4K+4K+(4K+256). All of them can be operated independently. It has the following modes:

- 1) MCU running at ZRAM1, while DMA[M] read B1 and DMA[N] write B2. Vice versa.  
M=4,5,6; N=4,5,6 ; M!=N.
- 2) MCU is running at ZRAM1, while DMA[M] read B2 and DMA[N] write ZRAM3. Vice versa.  
M=4,5; N=4,5 ; M!=N.
- 3) MCU is running at ZRAM1, while DMA[M] read B1 and DMA[N] write ZRAM3. Vice versa.  
M=4,5; N=4,5 ; M!=N.
- 4) MCU running at ZRAM1 or ZRAM2 or ZRAM3.

**IPM and IDM**

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

PM/DM can be accessed by MCU, DSP, DMA1, DMA2, DMA4 and DMA5.

When DSP is accessing the high (low) 8Kbytes, MCU/DMA1,2,4,5 can access low (high) 8K bytes at the same time.

### 3.5 USB2.0 SIE

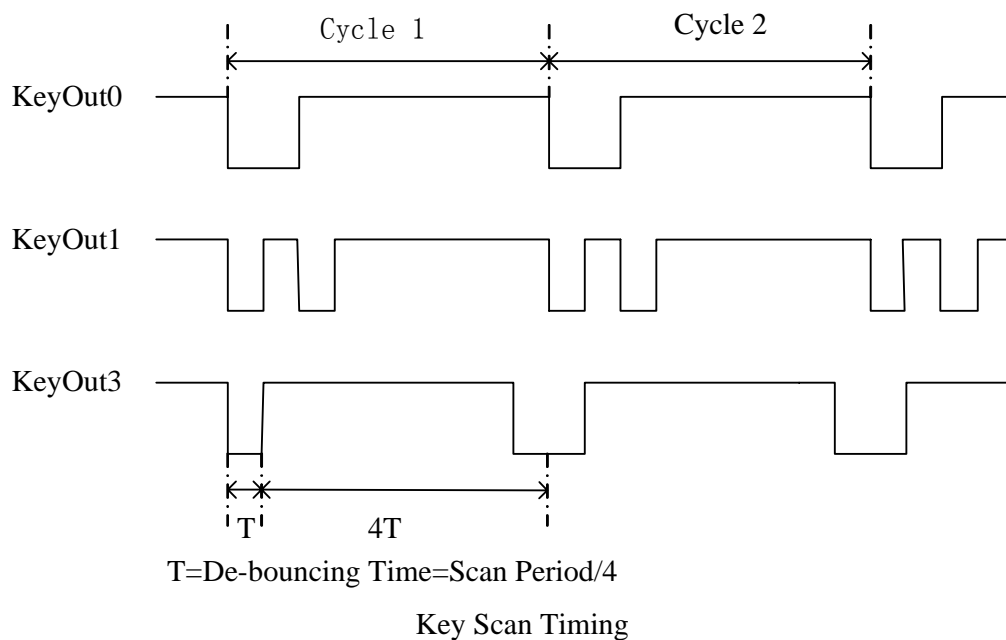
The Actions USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. In high-speed mode this device is capable of transmitting or receiving data up to 480Mbps. This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

### 3.6 NAND Flash /SMC Controller

The NAND Flash/SMC controller is a configurable interface to external NAND Flash/SMC. The highly configurable and flexible interface can attach to using most of readily available NAND Flash device. The flash data bus can be configured to be 8-bit access.

The controller automatically generates the Reading, Programming and Other commands timing by proper CLE, ALE and CE controls. So reliable data transferring between the Int. RAM and ext. Flash by MCU or DMA is available.

### 3.7 Key Scan Interface



**Figure 4: Key Scan Timing**

### 3.8 General Purpose IO Ports

ATJ2111A has GPIOA, GPIOB, GPIOC, GPIOE and GPIOF. Most of them are multiplexed function pins as the following table shows:

**Table 2: GPIO Modes**

GPIO	F1(CE0S=H default)
GPIO_A0	GPIO_A0
GPIO_A1	GPIO_A1
GPIO_A2	GPIO_A2
GPIO_A3	CE5-/GPIO_A3
GPIO_A4	CE2-/GPIO_A4
GPIO_B0	KEYI0/GPIO_B0/CE3-
GPIO_B2	KEYO0/GPIO_B2/CE4-

GPIO_B3	KEY01/GPIO_B3/SIRQ-
GPIO_C0	GPIO_C0/I2C_SCL
GPIO_C1	GPIO_C1/I2C_SDA
GPIO_E0	GPIO_E0/KEYI2
GPIO_E1	GPIO_E1/KEYI3
GPIO_F7	GPIO_F7

### 3.9 HOSC/PLL

ATJ2111A supports 24Mhz crystal which is the system clock source.

A low jitter PLL referenced to 24MHz is used to generate clock for DSP and for serial communication protocols such as USB, UART, etc. The clock used in serial communications is 48MHz. Another PLL referenced to 24MHz is used to generate 22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz and 24.576MHz for audio sequence of 48Khz.

### 3.10 PMU/DC-DC

#### 3.10.1 DC-DC converters and regulators

There are two on-chip DC-DC converters and two Regulators. Both of the two DC-DC converters work in boost mode for different input voltage, and can work in PFM or PWM modulation for different load current.

Table 3: Power mode configuration

PWRM	DC5V>4.3V	DC-DC1	Regulator1	DC-DC2	IO_VDD	Regulator2	Description
0	0	Boost	N	Boost	VDD	N	1 Alkaline/NIMH, 2 Inductor
0	0	Boost	N	N	GND	From VCC	1 Alkaline/NIMH, 1 Inductor
X	1	N	Y	N	-	From VCC	USB

#### 3.10.2 Battery monitor

There is a low speed 6-bit A/D for Battery monitor and wire control.

The relationship between battery type and the A/D input range is:

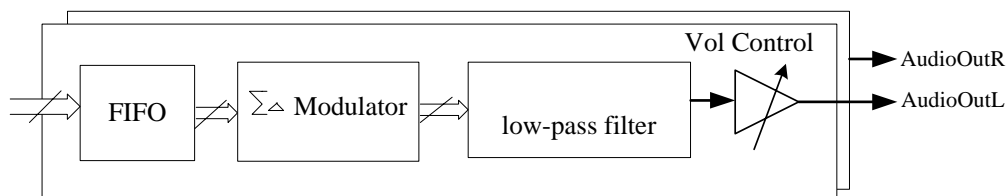
**Table 4: Relationship between Battery Type and A/D Input Range**

Battery type	Internal Voltage divider for battery	Battery Voltage Range
1 Alkaline/NIMH	1	0.7-1.5

### 3.11 A/D, D/A, IIS Port and Headphone Driver

#### 3.11.1 D/A Interface

ATJ2111A's internal D/A is an on-chip Sigma-Delta Modulator, a high performance D/A is composed of it. The D/A interface support 8-level play back FIFO (16 X 24-bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256XFS clock for over-sampling, while 24.576MHz supports 48K/32K/24K/16K/12K/8K Hz with 256XFS for over-sampling.



**Figure 5: D/A Block Diagram**

Internal D/A can drive earphone directly and the pin PAVCC need a bypass capacitor about 100uF to eliminate the “PENG” when D/A is powered on or off. D/A includes an analog mixer, reference to the ADDA block diagram.

#### 3.11.2 A/D

The internal microphone amplifier has gain for recording. The VMIC pin is the power supply (2.2V) for microphone.

The audio A/D is a 21 bits sigma delta Analog-to-Digital Converter. Its input source can

be selected from MIC amplifier or external FM, and it has two FIFOs.

The FS Supports 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.

## 4

## Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Table 5: Absolute Max Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.6	-0.3~2.0	V
	VCC	3.0	-0.3~3.6	V
Input voltage	V <sub>I</sub>		-0.3~3.6	V
Storage temperature	T <sub>stg</sub>	25	-65~150	°C

Note:

1. T<sub>0</sub> = 25°C (Operating Temperature)
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

### 4.2 Capacitance

Table 6: Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f <sub>c</sub> = 1 MHz		15	pF
I/O capacitance	C <sub>IO</sub>	Unmeasured pins returned to 0 V		15	pF

Note: T<sub>0</sub> = 25°C, VCC = 0 V.

### 4.3 DC Characteristics

Table 7: DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	$V_{OH}$	$I_{OH} = -6 \text{ mA}$	2.4			V
Low-level output voltage	$V_{OL}$	$I_{OL} = 6 \text{ mA}$			0.4	V
High-level input voltage	$V_{IH}$		$0.6 \cdot V_{CC}$		$V_{CC} + 0.6$	V
Low-level input voltage	$V_{IL}$		-0.3		$0.4 \cdot V_{CC}$	V
Input leakage current	$I_{LI}$	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC}, 0 \text{ V}$		$\pm 25$		$\mu\text{A}$
Tri-State leakage current	$I_{LO}$	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC}, 0 \text{ V}$		$\pm 25$		$\mu\text{A}$
GPIO Drive	$I_{drive1}$			5		mA
	$I_{drive2}$			10		mA
	$I_{drive3}$			15		mA

**NOTES:**

- $T_o = -10$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.6 \text{ V}$ ,  $V_{CC} = 3.0 \text{ V}$
- GPIO should not be floating in order to reduce the standby current, refer to the Application Note for the detailed information.
- There are three types of GPIO drives ranging from 5mA to 15mA, refer to the Section 2.2 Pin Definition for the detailed information.

## 4.4 AC Characteristics

$T_o = -10$  to  $+70^\circ\text{C}$

### 4.4.1 AC Test Input Waveform





Figure 6: AC Test Waveform

#### 4.4.2 AC Test Output Measuring Points

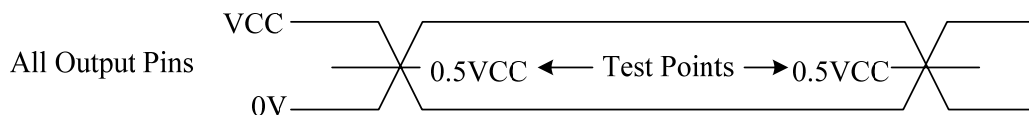


Figure 7: AC Test Output Measuring Points

#### 4.4.3 Reset Parameter

Table 8: Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	$t_{WRSL}$	RESET# pin	50	—	us

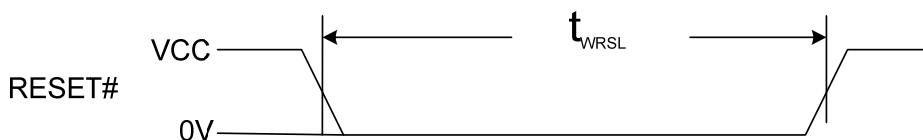


Figure 8: Reset Parameter

#### 4.4.4 Initialization Parameter

Table 9: Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET# )	$t_{ss}$		—	61.04	us
Output delay time (from RESET# )	$t_{od}$		61.04	—	us

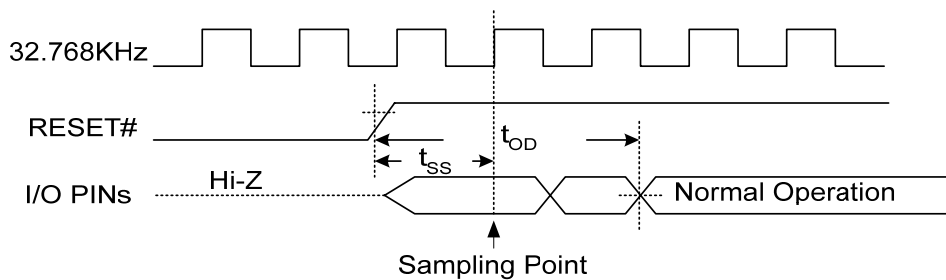


Figure 9: Initialization

#### 4.4.5 GPIO Interface Parameter

Table 10: GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	$t_{GPIN}$	Normal operation	$11/f_{mcuclk}$		s
GPIO output rise time	$t_{GPRISE}$		5	50	ns
GPIO output fall time	$t_{GPFALL}$		5	50	ns
Output level width	$t_{GPOUT}$		$11/f_{mcuclk}$		s

Notes 1.  $f_{mcuclk}$  is the frequency that MCU is running upon.

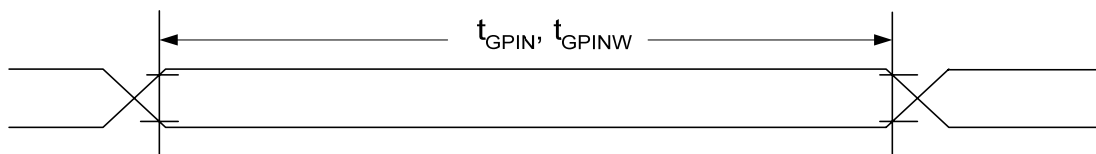


Figure 10: Input Level Width



Figure 11: Output Rise/Fall Time

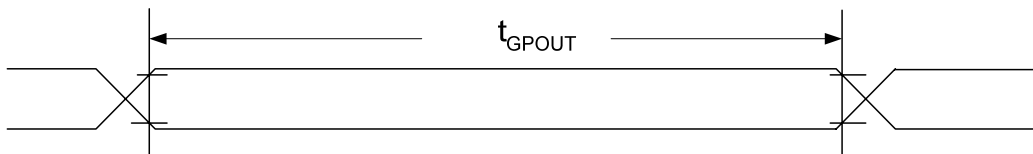


Figure 12: Output Level Width

#### 4.4.6 Ordinary ROM Parameter

Table 11: Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address) <sup>Note</sup>	$t_{ACC}$	HOSC=24MHz	90		ns
Data access time (from CEx#) <sup>Note</sup>	$t_{CE}$	HOSC=24MHz	90		ns
Data input setup time	$t_{DS}$	HOSC=24MHz	40		ns
Data input hold time	$t_{DH}$	HOSC=24MHz	15		ns

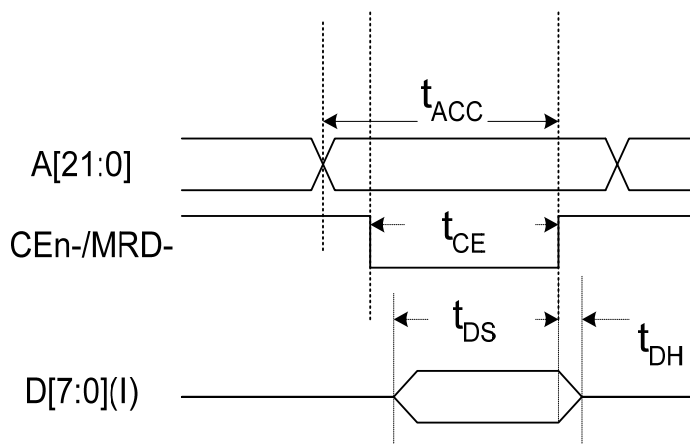


Figure 13: Ordinary ROM

#### 4.4.7 External System Bus Parameter

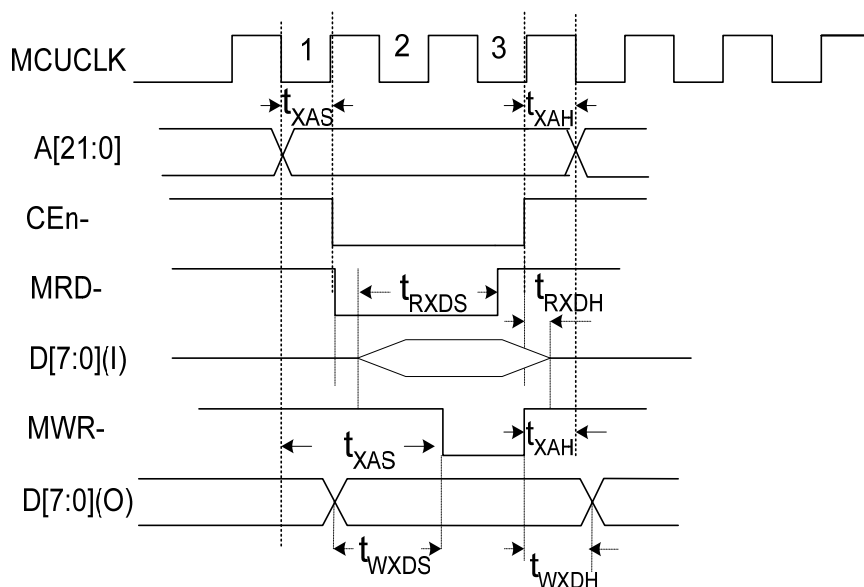


Figure 14: External System Bus Parameter

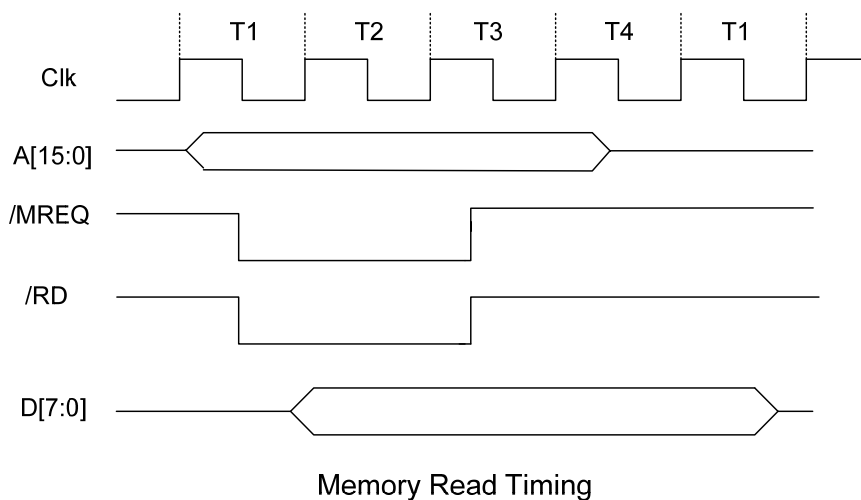
Table 12: External System Bus Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal) <sup>Note 1, 2</sup>	$t_{XAS}$	Memory Read	10		ns
	$t_{XAS}$	Memory Write	10		ns
Address hold time (from command signal) <sup>Note 1, 2</sup>	$t_{XAH}$		5		ns
Data output setup time (to command signal) <sup>Note 1</sup>	$t_{WXDS}$		20		ns
Data output hold time (from command signal) <sup>Note 1</sup>	$t_{WXDH}$		10		ns
Data input setup time (to command signal) <sup>Note 1</sup>	$t_{RXDS}$		20		ns
Data input hold time (from command signal) <sup>Note 1</sup>	$t_{RXDH}$		10		ns

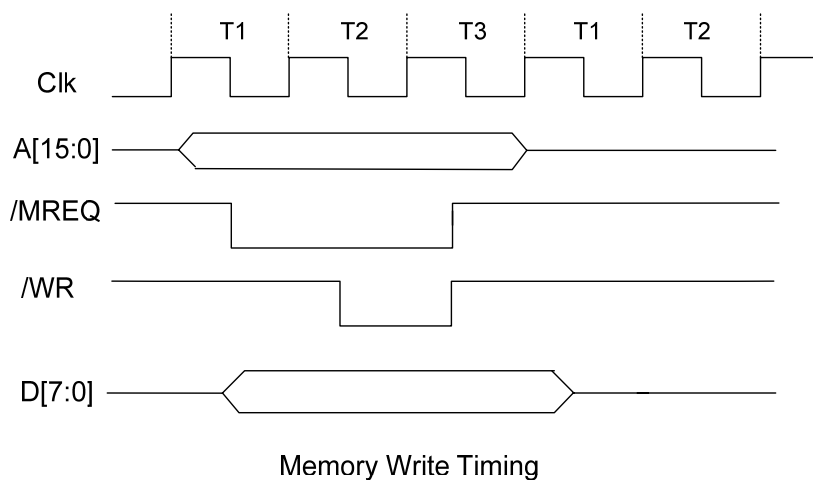
Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2.  $T \text{ (ns)} = 1 / f_{MCUCCLK}$

### 4.4.8 Bus Operation



**Figure 15: Memory Read Timing**



**Figure 16: Memory Write Timing**

### 4.4.9 A/D Converter Characteristics

(TA = -10 - +70°C, VDD = 2.0 V, VCC = 3.3V, Sample Rate=48KHz)

**Table 13: A/D Converter Characteristics**

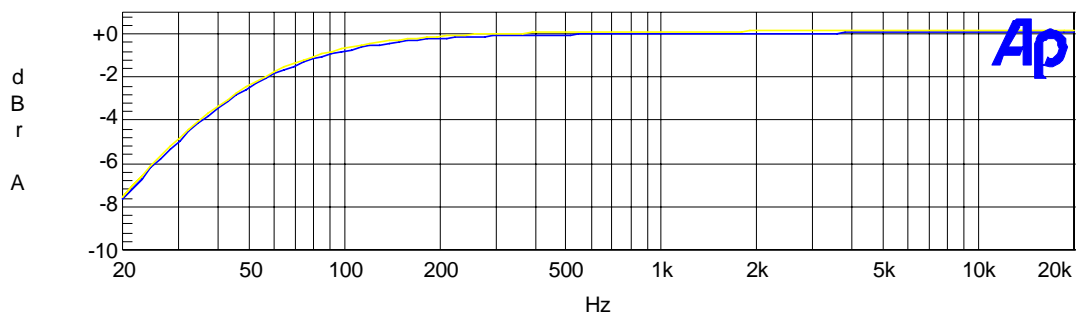
Characteristics	Min	Typ.	Max	Unit
Dynamic range		87.0		dB
Total Harmonic Distortion + Noise		85.0		dB
Frequency Response (20-13KHz)			±0.98	dB
Full Scale Input Voltage(Gain=0dB)		2.7		Vpp

#### 4.4.10 Headphone Driver Characteristics Table

**Table 14: Headphone Driver Characteristics**

 (T<sub>o</sub> = -10 ~ +70℃, VDD = 1.6 V, VCC = 3.0 V, Sample Rate=32KHz, Volume Level=0x1F)

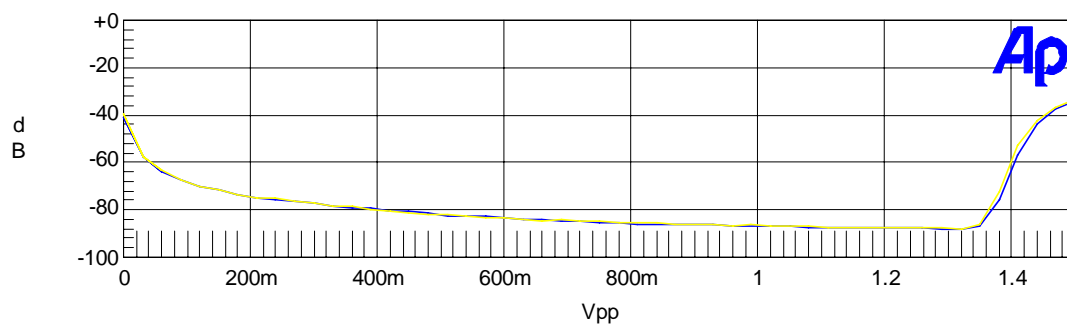
Characteristics	Min	Typ	Max	Unit
Dynamic Range -60 dBFS Input		-87		dB
Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		Vpp
Inter channel Gain Mismatch(1KHz)		-66		dB



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

audio2722.at27

**Figure 17: Frequency Response Diagram of Headphone Driver**



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THd+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THd+N Ratio	Left	

audio2722.at27

**Figure 18: THD + N Amplitude Diagram of Headphone Driver**

#### 4.4.11 LCM Driver Parameter

## LCM Interface Timing

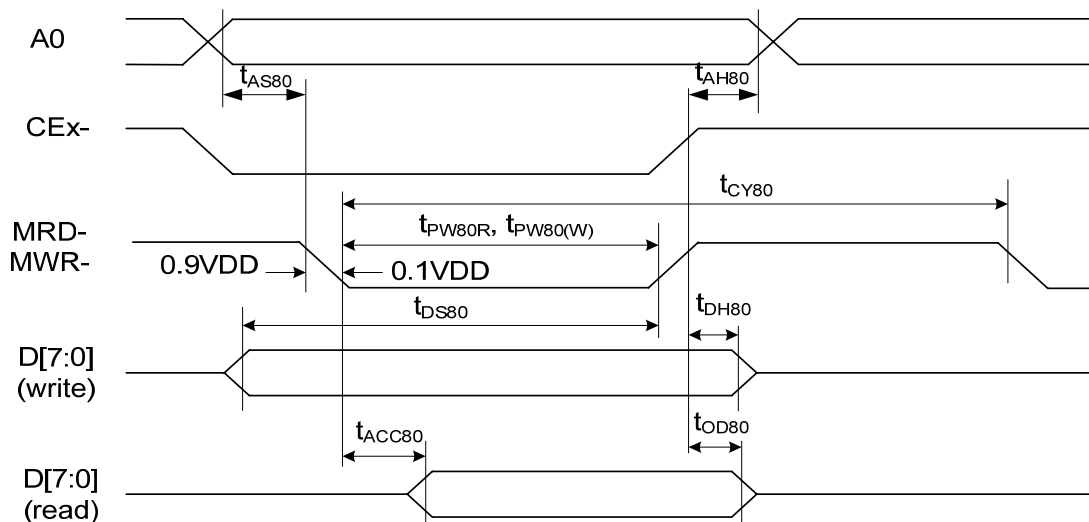


Figure 19: LCM Interface Timing

Table 15: LCD Driver Parameter

Parameter	Symbol	Condition	Typ	Unit
Data access time(write)	$t_{PW80(W)}$	HOSC=24MHZ	29	ns
Data access time (Read)	$t_{PW80(R)}$	HOSC=24MHZ	67	ns
Write cycle time	$t_{CY80(W)}$	HOSC=24MHZ	407	ns
Read cycle time	$t_{CY80(R)}$	HOSC=24MHZ	284	ns
Data setup time	$t_{DS80}$	HOSC=24MHZ	79	ns
Data hold time	$t_{DH80}$	HOSC=24MHZ	8	ns
Address setup time	$t_{AS80}$	HOSC=24MHZ	11	ns
Address hold time	$t_{AH80}$	HOSC=24MHZ	11	ns
Read access time	$t_{ACC80}$	HOSC=24MHZ	13	ns
Data input hold time	$t_{OD80}$	HOSC=24MHZ	8	ns



## 5 *Soldering Conditions*

### 5.1 Recommended Soldering Conditions

**Table 16: Soldering Conditions for Surface-Mount Devices**

Soldering Process	Soldering Conditions
Infrared Ray Reflow	Peak package's surface temperature: 235℃ (Lead) or 260℃ (Lead Free)
	Reflow time: 30 seconds or less (210℃ or more)—(Lead) or 60 seconds or less (217℃ or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

**Note:**

The maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

**Caution:**

Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

### 5.2 Precaution against ESD for Semiconductors

When the strong electric field is exposed to a MOS device, the destruction of the gate

oxide may occur and then it can ultimately degrade the device operation. Measures must be taken to stop the generation of static electricity as many as possible, and it is a must to quickly dissipate the static electricity when it occurs. Environmental control must be adequate enough. Humidifier should be used when it is dry. Recommend to avoid using insulators, which may easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container or a static shielding bag or objects made from conductive material. All test and measurement tools including work bench and floor should be grounded. The operator shall be grounded by using wrist strap. Semiconductor devices shall not be touched with bare hands. Similar precautions shall be taken for PW boards with semiconductor devices on it.

### 5.3 Handling of Unused Input Pins for CMOS

The cause for no connection to CMOS device inputs can be the malfunction. If no connection is provided for the input pins, the possible cause is that an internal input level may be generated due to noise, etc., which results in malfunction. CMOS devices behave differently from Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin shall be connected to VDD or GND with a resistor, if it is considered to have the possibility of being an output pin. All handling related to the unused pins must be judged device by device and follows the related specifications governing the devices.

### 5.4 Status before Initialization of MOS Devices

Power-on does not necessarily define the initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned on, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after the power-on.

6

ATJ2111A Package Drawing

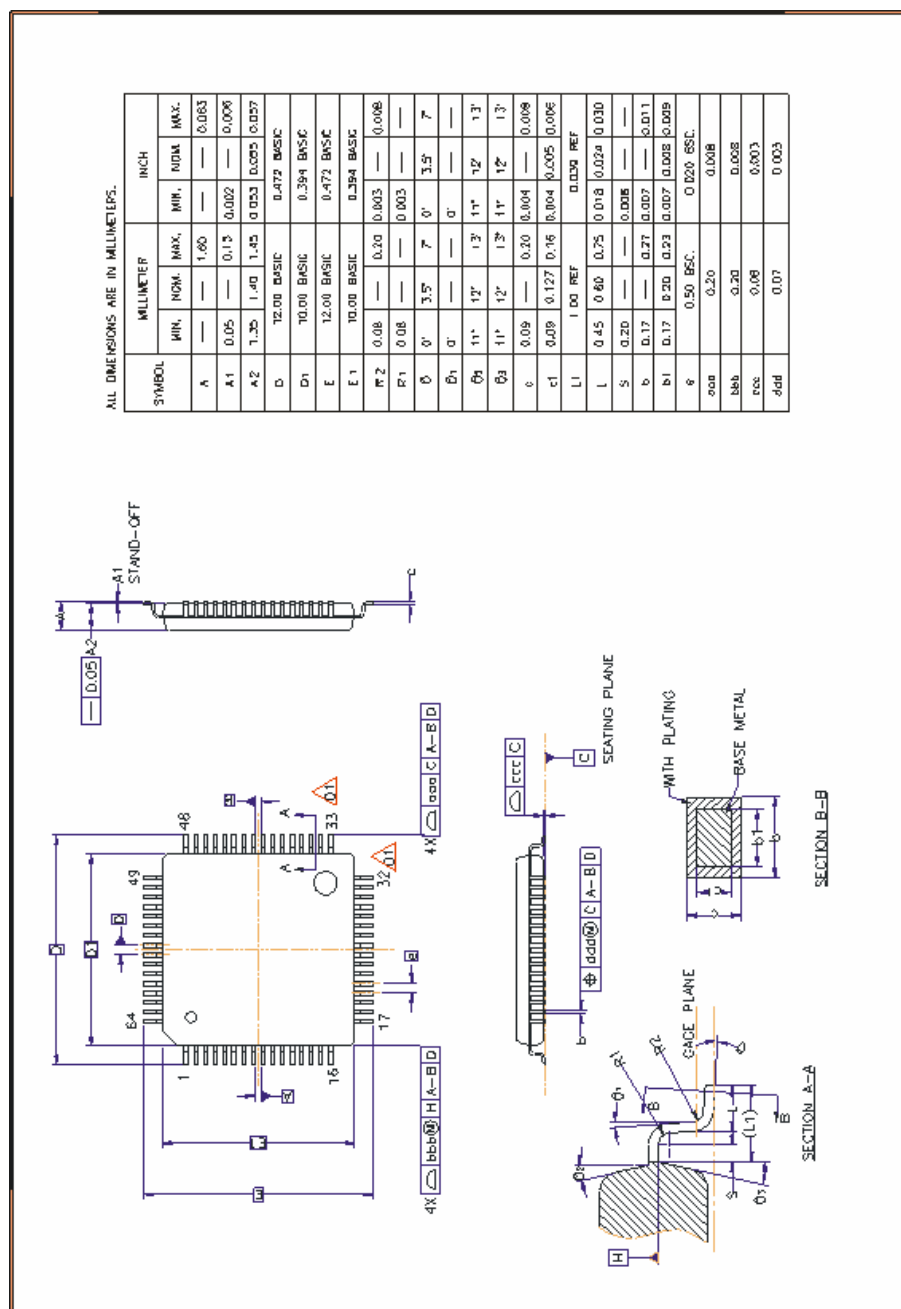


Figure 20: ATJ2111A Package Drawing

7

*Appendix*

---

**7.1 Acronym and Abbreviations**

ACK—Acknowledgement

ADC—Analog Digital Converter

ATAIRQ—Advanced Technology Attachment Interrupt Request

CTC—Counter/Timer Channels

DAC—Digital Analog Converter

DMA—Direct Memory Access

DRQ—Data Request

DST—Destination

ECC—Error Correction Code

EM—External/Extended Memory

FIFO—First In First Out

HIP—Host Interface Port

HOSC—High Frequency Oscillator

IDM—Internal Data Memory

IPM—Internal Program Memory

IRQ—Interrupt Request

IR—Infra-red

LOSC—Low Frequency Oscillator

MIC—Microphone

NAK—Negative Acknowledgement

PLL—Phase Locked Loop

RTC—Real Time Clock

RB—Ready/Busy

SIRQ—System external Interrupt Request

SPDIF—Sony/Philips Digital Interface

SPI—Serial Port Interface

SRC—Source

TC—Transmit Complete

UART—Universal Asynchronous Receiver/Transmitter

**Actions Semiconductor Co., Ltd.**

**Address: Bldg.15-1, NO.1, HIT Rd., Tangjia, Zhuhai, Guangdong, China**

**Tel: +86-756-3392353**

**Fax: +86-756-3392251**

**Post Code: 519085**

**<http://www.actions-semi.com>**

**Business Email: [mp-sales@actions-semi.com](mailto:mp-sales@actions-semi.com)**

**Technical Service Email: [mp-cs@actions-semi.com](mailto:mp-cs@actions-semi.com)**